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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/442,363	11/17/1999	LARRY PEARLSTEIN	(DSML)HA-80(	5725

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EXAMINER	
PARSONS, CHARLES E	
ART UNIT	**PAPER NUMBER**
2613	9

DATE MAILED: 04/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/442,363	PEARLSTEIN ET AL.	
	Examiner	Art Unit	
	Charles E Parsons	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 2/09/2004 have been fully considered but they are not fully persuasive. In view of the arguments as they apply to the 103 rejection in view of the prior art taken alone, the Examiner agrees with the Applicant and withdraws that particular rejection. However, the Examiner stands behind his rejection based upon the admitted prior art in view of Purcell.

2. First the Applicant misinterpreted the rejection and is attempting to twist the facts. The rejection clearly points out that the non-memory intensive step of the VLD has been done in hardware long before the current invention as admitted by the Applicant. What the Examiner lacked by taking the Admitted prior art alone was supplying the process image data to a programmable processor and performing an additional image decoding operation using the processed image data. According to Applicants own specification, the additional step is the motion compensation step. At the time the invention was made, it was well known in the art that the motion compensation step is a memory intensive step. The Examiner further pointed out that Purcell clearly teaches separating the motion compensation step which again is the memory intensive step and implementing it in software within a dedicated core processor. The Applicant continues to assert, incorrectly, that the Examiner suggested using dedicated non-programmable hardware for the memory intensive step of motion compensation when this in indeed is not the case.

As for the Examiners alleged argument that any and all combinations of Software/hardware decoding combinations were obvious, the Examiner already showed him evidence of such obviousness by citing the references now included in this action which he admitted to not having reviewed even though the Examiner gave them to him upon completion of the interview. At the time the invention was made, a person of ordinary skill in the art, knew that a piece of hardware, in this case a chip, must be programmed in order to operate. The programming can be hard coded meaning that once the chip is programmed as in an EPROM, it cannot be dynamically programmed during implementation. Thus the creation of a dedicated hardware processor that is only programmable upon initialization of the chip also known in the

art as a dedicated hardware processor. Further a person of ordinary skill in the art, knew that a programmable processor such as a CPU processor is capable of executing software commands as long as the proper compiler was installed. Therefore, separation of individual parts of a system and implementing some of them in hardware and some in software may be construed as design choice, and is well within the scope of one of ordinary skill in the art.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants admitted prior art in view of Purcell.

Claim 1, 19. A method of decoding encoded image data comprising the steps of:

operating a decoder circuit implemented in hardware to perform at least one non-memory intensive image decoding operation to generate, from the encoded image data, a first set of processed image data, the at least one non-memory intensive image decoding operation being an operation in the group of operations consisting of a variable length decoding operation an inverse scan conversion operation, and an inverse quantization operation, See figure 1 of Applicants admitted prior art as well as Purcell column 3 lines 60-65

supplying the first set of processed image data generated by the decoder circuit to a programmable processor; and (See column 3 line 66, some Purcells Processors are

programmable. See columns 33-156 wherein he shows the code used to program his processors.)

operating the programmable processor to perform at least one additional image decoding operation using the first set of processed image data. While the applicants prior art of record does not appear use a programmable processor to separate the memory intensive functions of the decoder, Purcell clearly does, See column 3 line 66. A motion compensation step is an additional step and it is done in a separate processor from the non-memory intensive steps. At the time the invention was made, it was well known in the art that programmable processors could be used to carry out video data manipulations such as MPEG decoding. It was also well known that in order to reduce processing times, it was advantageous to split the decoding function into different blocks and assign the tasks to different processors as taught by Purcell. Therefore it would have been obvious to one of ordinary skill in the art, to use a dedicated processor for the memory intensive steps in order to reduce the amount of time it takes to decode the image.)

Claim 2: The method of claim 1, wherein the step of operating the decoder circuit, includes the step of performing at least two additional operations from the group of operations consisting of a variable length decoding operation, an inverse scan conversion operation, an inverse quantization operation, an inverse discrete cosine transform operation, and a data reduction operation, the two additional operations being different from said at least one non-memory intensive operation. (See admitted prior art figure 1))

Claim 3 and 4. The method of claim 1, wherein the step of operating the decoder circuit further includes: operating the decoder circuit to perform a data reduction operation. (This is the purpose of decoders thus not a patentable element)

Claim 5. The method of claim 2, wherein the step of operating the programmable processor to perform at least one additional image decoding operation includes the step of: operating the programmable processor to perform a motion compensated prediction operation. (See column 7 lines 63-65)

Claim 6: The method of claim 5, wherein the step of operating the programmable processor to perform at least one additional image decoding operation further includes the step of: operating the programmable processor to combine decoded image data produced by performing the motion compensated prediction operation with decoded residual image data to produce a set of decoded image data representing reconstructed pixels. (See Purcell figure 1)

Claim 7. The method of claim 1, wherein the step of operating the programmable processor to perform at least one additional image decoding operation includes the step of:
operating the programmable processor to combine decoded image data produced by performing a motion compensated prediction operation with decoded intra-coded image data to produce a set of decoded image data representing a complete frame. See Purcell Figure 1)

Claim 8. The method of claim 2, wherein the programmable processor is coupled to a graphics processor, the method further comprising the step of:
operating the graphics processor to perform a motion compensated prediction operation using data included in the first set of processed data. (See Purcell figure 2)

Claim 9. The method of claim 8, wherein the step of operating the programmable processor to perform at least one additional image decoding operation further includes the step of: operating the programmable processor to combine decoded image data produced by performing the motion compensated prediction operation with decoded residual image

data to produce a set of decoded image data representing reconstructed pixels. (See figures 1,2 and 3 of Purcell)

Claim 10, 11, 12, 13. The method of claim 8, further comprising the step of storing in the decoder circuit multiple sets of context information, each set of stored context information corresponding to a different one of a plurality of encoded data streams processed by the decoder circuit. (See Purcell column 17 line 44 through column 18 line 16.)

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles E Parsons whose telephone number is 703-305-3862. The examiner can normally be reached on M-TH 7AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Kelley can be reached on 703-305-4856. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CEP

CHRIS KELLEY
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